



Name : .....

Roll No. : .....

Invigilator's Signature : .....

**CS/M.Tech(CSE)/SEM-1/CSEM-105/2011-12  
2011**

**COMPUTER ARCHITECTURE**

Time Allotted : 3 Hours

Full Marks : 70

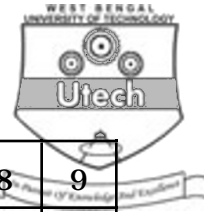
*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words  
as far as practicable.*

**GROUP - A**

Answer any *three* of the following.  $3 \times 14 = 42$

1. a) Define speedup and efficiency ? 2
- b) A 4-segment pipeline has clock cycle time 30ns in each sub operation. If we have to execute 120 complete tasks then what will be the speedup and efficiency of the pipeline ? 3
- c) SUB  $R_3, R_0, R_1$  ;  
MUL  $R_4, R_3, R_0$  ;  
DIV  $R_0, R_4, R_1$  ;  
SUB  $R_1, R_4, R_0$  ;  
Store  $R_1, X$  ;  
  
Check out the data hazards occurred in the given set of instructions, how many clock cycles are required to complete the execution of the instruction having a 4 stage pipeline ? ( only MUL and DIV instruction requires 3 clock rest of the instructions require only 1 clock cycle ) 4
- d) How can you eliminate hazards by using compiler technology ? 5



2.

	1	2	3	4	5	6	7	8	9
$S_1$	X								X
$S_2$		X	X					X	
$S_3$				X					
$S_4$					X	X			
$S_5$							X	X	

It is the reservation table of pipeline of  $P_1$  what will be the MAL value for the pipeline then what is the throughput and efficiency of the pipeline  $P_1$ . 14

3. a) What are the main issues associated with multiprocessor caches and how might you solve them ? 2
- b) What is the difference between Write-Through and Write-Back caches ? Explain advantages and disadvantages of each. 4
- c) Cache size is 64 KB, Block size is 32 B and the cache is two-Way set associative. For a 32-bit physical address, give the division between Block offset, Index and Tag. 2
- d) What is MESI ? 2
- e) What is snooping cache ? 4



4. a) Explain how directory protocol helps in maintaining cache coherence. 6
- b) What is strip mining ? 3
- c) What is balanced vector/scalar ratio ? Why is it so important in supercomputing ? 2 + 3
5. a) Write down the difference between vector and scalar processors ? 3
- b) What are the components of the vector processors ? How do they help in implementing a vector processor ? 7
- c) What are the advantages and disadvantages of using a vector processor ? 4

**GROUP - B**

Answer any *two* of the following.  $2 \times 14 = 28$

6. a) Draw the diagram of a  $8 \times 8$  Omega NW built with  $2 \times 2$  switching elements.
- b) How is an Omega NW configured to implement the shuffle-exchange operation ? 9 + 5
7. a) Suppose you have  $n^r$  processors at your disposal. You have an algorithm like the matrix multiplication which has  $O(n^3)$  time complexity. Can you get time complexities  $O(n^{3-r})$  for  $r > 3$  ? What interesting event would have occurred had this been achievable ?
- b) Show diagrammatically how a  $2 \times 2$  switch can be reconfigured to operate in various modes it can operate. 7 + 7



8. a) From two 3-cubes show how you can configure a 4-cube.

b) Explain the working of parallel sorting algorithms on the following seven elements :

11 22 12 17 33 21 23 6 + 8

9. a) Illustrate the matrix multiplication procedure on a Boolean Cube consisting of  $n^3$  processing elements.

b) How is an Omega NW different from a delta NW ?

12 + 2

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