



Name : .....

Roll No. : .....

Invigilator's Signature : .....

**CS / B.TECH(ICE / EIE(O) / SEM-6 / EI-602 / 2011**

**2011**

**MICROPROCESSOR BASED SYSTEM**

Time Allotted : 3 Hours

Full Marks : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words as far as practicable.*

**GROUP – A**

**( Multiple Choice Type Questions )**

1. Choose the correct alternatives for any *ten* of the following :

10 × 1 = 10

i) An 8255 is interfaced with 8086 the port A address is 0740H. What will be the address of port C ?

- |          |           |
|----------|-----------|
| a) 0740H | b) 0744H  |
| c) 0745H | d) 0746H. |

ii) What is the vector location for INT33 ?

- |          |           |
|----------|-----------|
| a) FF48H | b) 0033H  |
| c) 0132H | d) 0084H. |



iii) Which registers are used as the base location for all executable instruction and stack ?

- a) CS & SS respectively
- b) DS & SP respectively
- c) ES & SS respectively
- d) None of these.

iv) Provision for software interrupts in 8086 is

- a) 32
- b) 256
- c) 64
- d) 128.

v) Address/data bus connected to odd memory bank is

- a) AD0-AD7
- b) AD8-AD15
- c) A16-A19
- d) any one of these.

vi) How many bits are obtained as an output from DAC 1208 chip ?

- a) 8
- b) 16
- c) 12
- d) 10.

vii) The SSO of 8088 microprocessor indicates

- a) status
- b) multiplexed status/address line
- c) multiplexed data/address line
- d) none of these.



- viii) Which of the following is wrong ?
- a) MOV SI, [ AX ]                      b) MOV DS, 0500
- c) MOV DS, AX                          d) XCHG AX, BX.
- ix) The size of the pre-decoding instruction queue in 8086 and 8088 microprocessor system are
- a) 8, 10
- b) 4, 6
- c) 6, 4
- d) there are no such a queue.
- x) The number of bytes of internal data RAM contained in 8051 is
- a) 256 bytes                              b) 512 bytes
- c) 1024 bytes                             d) 2K.
- xi) In "XCHG" instruction of 8085 microprocessor swaps the contents of registers are
- a) HL, DE                                 b) BC, DE
- c) DE, HL                                 d) BC, HL.
- xii) If ready pin is grounded, it will introduce ..... states into the bus cycle of 8085 microprocessor.
- a) wait                                      b) idle
- c) wait and remains idle                d) all of these.

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**GROUP – B**

**( Short Answer Type Questions )**

Answer any *three* of the following.  $3 \times 5 = 15$

2. Explain pipeline architecture. 5
  
3. Explain the function of SIM and RIM instruction in 8085 ? 5
  
4. What do you mean by addressing mode ? What are the different addressing modes supported by 8086 ? Explain each of them with suitable examples. 1 + 4
  
5. Describe the function of different bits of PCON register regarding 8051  $\mu$ C. 5
  
6. Discuss how a wave of variable duty cycle can be generated using suitable port bit of 8255 and BSR mode. 5



**GROUP – C**

**( Long Answer Type Questions )**

Answer any *three* of the following.  $3 \times 15 = 45$

7. a) Distinguish between Microprocessor 8086 and 8085.
- b) Write a program in 8086 to add the elements of two  $[ 3 \times 3 ]$  matrices in which 1st and 2nd matrix elements are stored from 2000 H and 3000 H offset address and the results store from 5000 H.
- c) What is the function of TEST, LOCK and pin in 8086 ?
- d) What are the addressing modes of the following instruction ?
- PUSH B, XTHL, MOV A,M.  $3 + 5 + 4 + 3$

8. a) What are the Off-set Address and Physical Address ? How is Physical address computed in case of 8086 ?
- b) Write a program in 8086 to count from 0 to 9 with a 1sec delay between each count. At the end of count 9, the counter should reset itself to 0 and repeat the sequence continuously. Use proper register pair to set up the delay and display each count at one of the O/P port. Assume system clock frequency as 1MHz.
- c) Describe the stack organization of 8086.  $5 + 6 + 4$



9. a) Interface a  $4k \times 8$  EPROM, one chip of  $8k \times 8$  RAM, Two chips of  $8k \times 4$  RAM with 8088. The map should be as follows :

i) EPROM : FFOOO H – FFFFF H

ii) one  $8k \times 8$  RAM : OOOOO H – O1FFF H

iii) Two  $8k \times 4$  RAM : O5OOO H – O6FFF H

b) Write a program to add the elements of two [  $3 \times 3$  ] matrices in which 1st and 2nd matrix elements are stored from 2000 and 3000 offset address and the results from 5000.

c) Pipeline architecture fasts the execution process in 8086 over 8085. Explain. 8 + 5 + 2

10. a) Draw and explain internal RAM organization of 8051 microcontroller.

b) Discuss the different bits of PSW register of 8051.

c) Discuss the addressing modes of 8051. 5 + 5 + 5

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11. Write short notes on any *three* of the following :  $3 \times 5 = 15$

- a) 8284
  - b) A/D converter interfacing
  - c) RS-232
  - d) 8251
  - e) N-Key rollover.
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