Name :


Roll No.


Invigilator's Signature :
CS/ B.Tech(EE-(N)/ EEE-(N)/ ICE(N)/ SEM-3/ EC(EE)-302/ 2011-12

## 2011

## DIGITAL ELECTRONIC CIRCUITS

Time Allotted: 3 Hours
Full Marks : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP - A
( Multiple Choice Type Questions )

1. Choose the correct alternatives for any ten of the following :

$$
10 \times 1=10
$$

i) The value of base $x$ for which (128) $)_{10}=(1003)_{x}$ is
a) 3
b) 4
c) 5
d) 6 .
ii) $\quad A+A^{\prime} B+A^{\prime} B^{\prime} C+A^{\prime} B^{\prime} C^{\prime} D+\ldots .$. is equal to
a) $A+B+C+\ldots$.
b) $A^{\prime}+B^{\prime}+C^{\prime}+D^{\prime}+\ldots$.
c) 1
d) 0 .
iii) The output of a gate is low if and only if all its inputs are high. It is true for
a) NOR gate
b) AND gate
c) NAND gate
d) X-NOR gate.
a) -256
b) -255
c) -128
d) -127 .
v) The Gray Code of ( 11001100$)_{2}$ is
a) 10101010
b) 1001100
c) 10111000
d) 1110001 .
vi) Which logic family has the better noise margin ?
a) ECL
b) DTL
c) MOS
d) TTL .
vii) A decoder with enable input can be used as
a) parity generator
b) encoder
c) demultiplexer
d) multiplexer
viii) A flip-flop is also known as
a) astable multivibrator
b) bistable multivibrator
c) a switch
d) none of these.
ix) The number of flip-flops required for a mod-16 ring counter is
a) 4
b) 8
c) 15
d) 16 .
x) A switch-tail ring counter is made by using a single $D$ flip-flop. The resulting circuit is
a) SR flip-flop
b) JK flip-flop
c) D flip-flop
d) T flip-flop.

xi) The number of comparisons carried out in a 4-bit flash type ADC is
a) 16
b) 15
c) 4
d) none of these.
xii) A decade counter counts up to
a) 9
b) 10
c) 11
d) 12 .

## GROUP - B <br> (Short Answer Type Questions )

Answer any three of the following. $3 \times 5=15$
2. Obtain the logic expression for a 3-input majority function and hence implement it using only NAND gates.
3. Design a full subtractor using two half-subtractors and one extra gate, if necessary.
4. Design a 4-bit comparator. Show the output functions only.
5. Design a D flip-flop into a JK flip-flop.
6. Design a mod-7 ripple counter using CLR lines of JK flipflops.

## GROUP - C

( Long Answer Type Questions )
Answer any three of the following. $3 \times 15=45$
7. a) Simplify the following function using $K$-map : $f=\sum m(0,5,8,10,11,14,15)+\sum d(3,13)$
b) Simplify the following function using tabular method : $f(A, B, C, D)=\sum m(0,2,3,6,7,8,10,12,13)$.

$$
7+8
$$

CS/B.Tech(EE-(N)/EEE-(N)/ICE(N)/SEM-3/EC(EE)-302/2011-12Rech
8. a) Implement the following function using multiplexer:
b) Explain race-around condition in SR flip-flop. Explain how this condition is avoided in JK flip-flop.
c) Draw the timing diagram of a 3-bit ring counter.

$$
4+(3+4)+4
$$

9. a) Design a 4-bit up/down synchronous serial counter using JK flip-flops and other necessary logic gates. Use one direction control input, D . If $\mathrm{D}=0$, the counter will count up and for $\mathrm{D}=1$, the counter will count down.
b) Draw the circuit diagram of a mod-8 ripple counter using JK flip-flops. Draw the output waveforms also. Obtain the state table and hence show the corresponding state diagram. $7+8$
10. a) Draw a neat diagram for a weighted resistor type DAC and explain its operation.
b) Describe the operation of successive approximation type ADC . How many clock pulses are required in worst case for each conversion cycle of an 8-bit SAR type ADC ?

$$
7+(7+1)
$$

11. Write short notes on any three of the following : $3 \times 5$
a) Switch-tail ring counter
b) Lock-out phenomena in counters
c) Parity checker/generator
d) PLA
e) Totempole configuration of TTL.
