EE-504C

MICROPROCESSORS AND MICROCONTROLLER

Time Allotted: 3 Hours | Full Marks: 70

The questions are of equal value.
The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP A
(Multiple Choice Type Questions)

1. Answer any *ten* questions. 10×1 = 10

(i) The number of register pairs of 8085 microprocessor is

(A) 3 (B) 2
(C) 4 (D) 5

(ii) Number of machine cycles in JMP is

(A) 3 (B) 2
(C) 4 (D) 5

(iii) Which of the following interrupt is both level and edge sensitive?

(A) RST 5.5 (B) RST 6.5
(C) RST 7.5 (D) TRAP

(iv) What is the restart address for RST 4?

(A) 0024H (B) 0020H
(C) 0028H (D) 0000H

(v) For 8255 PPI, the bi-directional mode of operation is supported in

(A) Mode 1 (B) Mode 2
(C) Mode 0 (D) either (A) or (B)

(vi) 8086 microprocessor is called a 16-bit microprocessor because

(A) data bus is 16 bit (B) address bus is 16 bit
(C) accumulator is 16 bit (D) its memory is 16 bit

(vii) The total I/O space available in 8085 microprocessor if used peripheral mapped I/O is

(A) 8 (B) 10
(C) 16 (D) 256

(viii) If the crystal with 8085 is 2 MHz, the time required to execute an instruction of 20 T- states are

(A) 20 μs (B) 10 μs
(C) 40 μs (D) 5 μs

(ix) The total memory space available in 8086 is

(A) 16 KB (B) 64 KB
(C) 1 MB (D) 256 KB

(x) T-States in "CALL" instruction of 8085 CPU are

(A) 13 (B) 18
(C) 10 (D) 7

(xi) 8259A interrupt controller controls how many interrupts

(A) 8 (B) 5
(C) 6 (D) 9

(xii) The _____ ensures that only one IC is active at a time to avoid a bus conflict caused by two ICs writing different data to the same bus.

(A) Control bus (B) Control instructions
(C) Address decoder (D) CPU

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. Explain the different types of addressing modes in 8085 with examples. 5

3. What is meant by subroutine? Briefly discuss the sequence of events that takes place while executing CALL instruction. 2+3

4. Write a program h based on 8085 CPU to find out the smallest number, starting from 2000 of 10 numbers and store result in 2200H. 5

5. (a) Explain the action of the bits of the control word register of 8255 PPI. 2
   (b) How is pipelining achieved in 8086 microprocessor? 3

6. (a) What is tri-state? Why is it important? 2
   (b) Can an input and an output port have same address? Justify. 3

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) What are the differences between a microprocessor and a microcontroller? 2+4+3+3+3
   (b) Discuss the memory organization of 8051 microcontroller. What is the function of program status word (PSW) in 8051?
   (c) What is the role of SFRs in 8051 microcontroller? Explain.
   (d) Write an 8051 assembly language program to add two 16 bit no.

8. (a) What are the main functions of BIU and EU? 4+4+4+3
   (b) What are the major segments in memory of an 8086 microprocessor system? What are their functions?

(c) What is minimum and maximum mode of 8086 microprocessor?

(d) With example state the generation of 20 bit physical address in context to 8086 μP.

9. (a) How many flag bits are there in 8085 microprocessor? Explain each of them.
   (b) Write an assembly language program to multiply two numbers of 8-bit data stored in the memory location XX00H and XX01H. Store the product in XX02H and XX03H. Use shift and add method.

10. (a) What do you mean by T-State, Machine Cycle and Execution Cycle?
   (b) Draw the Timing diagram of the following instruction stored in memory location starting from 80FF H- IN 50H
   (c) In a memory mapped I/O, how does a microprocessor differentiate between an I/O and memory?

11. Write short notes on any *three* of the following:
   (a) BSR mode of 8255
   (b) DMA controller.
   (c) RIM and SIM instructions of 8085
   (d) Flags of 8086 processor
   (e) Interfacing of external memory to 8051 microcontroller.