Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH (EIE)/SEM-4/CS-404 (EI)/2011

2011
COMPUTER ORGANISATION AND ARCHITECTURE

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

i) The logic circuit in ALU is

a) entirely combinational

b) entirely sequential

c) combinational-cum-sequential

d) none of these.

ii) Instruction eyele is

a) fetch & decode & execution

b) fetch-execution-decode.

c) decode-fetch-execution

d) none of these.

iii) Associative memory is a

a) pointer addressable memory

b) very cheap memory

c) content addressable memory

d) slow memory.

iv) A full subtractor can be designed with a full adder by

a) only changing the circuit

b) adding a not with sum input

c) adding a not with carry input

d) none of these.

v) The page and frame size

a) should be equal

b) need not be equal

c) page size > frame size

d) frame size > page size.

vi) MAR stands for

a) Memory Address Register

b) Memory Abstract Register

c) Memory Activity Register

d) None of these.

vii) Principle of locality is justified in the use of

a) Daisy chaining

b) DNA

c) Interrupts

d) Cache Memory.

viii) A "hit" is considered when

a) word is found in cache

b) word is not found in cache

c) word is found in virtual memory

d) word is not found in virtual memory.

ix) How many address bits are required for a 1024×8 memory ?

a) 5 b) 10

c) 1024 d) none of these.

x) Delayed branching is related to

a) Pipeline hazard b) Pipeline remedy

c) both (a) & (b) d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. a) What is virtual memory ? Why is it called virtual ? Write the advantages of virtual memory. 3

   b) Explain speed-up & efficiency with respect to pipelined architecture. 2

3. a) What is cache memory ? Briefly describe the different mechanisms of writing into it. 3

   b) Represent $(-1.75)_{10}$ in IEEE 754 floating point format. 2

4. Explain the working of a Carry Look Ahead Adder with suitable example.

5. What are the different types of DMA controllers and how do they work ?

6. What are the different types of interrupt ? Give example. What is programmed I/O technique ?

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Classify different types of ROM and briefly describe them. What is flash memory ? Briefly describe the organisation of basic RAM cell. 3 + 1 + 3

   b) What is von Neumann architecture ? What is von Neumann bottleneck ? How can this be reduced ? 2 + 1 + 2

   c) What is vistual memory ? Why is it called virtual ? 1 + 1

   d) What is tertiary memory ? 1

8. a) Using Booth's algorithm multiply (-3) and (-5) upto 5 digits. Show each step. 6

   b) Evaluate the following statement using zero, two and three address machine :

   Z = (M + N) * (P + Q). 6

   c) Explain Flynn's classification w.r.t. computer architecture. 3

9. a) Explain the difference between associative and set-associative cache mapping techniques. 4

b) With the help of given information, determine the size of subfields (in bits) in the address of Direct, Associative and Set Associative mapping :

i) 512 MB main memory & 2MB cache memory.

ii) Address space of processor is 256 MB

iii) Block size is 256 bytes.

iv) There are 16 blocks in cache set. 6

c) Briefly explain two write policies : write through and write back for cache design. Explain the advantages and disadvantages of both the methods. 5

10. a) Briefly explain combinational ALU organisation. 5

b) What are instruction and arithmetic pipelines ? 3

c) Describe pipeline hazards. 5

d) What do you mean by paging ? 2

11. Write shot notes on any *three* : 3×5

a) DMA based data transfer operation

b) Different I/O techniques

c) SIMD *vs* MIMD

d) Instruction cycle *vs* Machine cycle.