ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2008

MICROPROCESSOR AND MICROCONTROLLER

SEMESTER - 4

Time : 3 Hours] [Full Marks : 70

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

i) The machine cycles involved in the execution of the instruction SUB M are

a) Opcode fetch b) Opcode fetch + Memory write

c) Opcode fetch + Memory read d) None of these. ☐

ii) How many output devices can be identified by the MPU using Memory mapped I/O ?

a) 256 b) 255

c) 65536 d) 128. ☐

iii) The flags affected by the instruction DCX B are

a) carry, zero b) all except carry

c) both (a) & (b) d) none of these. ☐

iv) For 8257 controller ..... is the highest priority channel by default.

a) CH-0 b) CH-1

c) CH-2 d) any channel. ☐

v) The number of I/O ports available in 8051 are

a) 4 b) 3

c) 2 d) None of these. ☐

vi) When a subroutine is called the address of the instruction next to CALL is saved in

a) Stack pointer register

b) Program counter register

c) Stack

d) Combination of flag and Accumulator. ☐

vii) The port of 8255 which can be used in BSR mode is

a) Port A only b) Port B only

c) Port C only d) None of these. ☐

viii) 8254 timer controller support ..... modes of operation.

a) 3 b) 5

c) 6 d) 2. ☐

ix) The number of register banks in 8051 are

a) 4 b) 3

c) 8 d) 2. ☐

x) To operate 64 of priority interrupt level, ... interrupt controller 8259A is needed.

a) one b) eight

c) nine d) two. ☐

xi) The maximum operating frequency of 8254 is

a) 2 MHz b) 3 MHz

c) 5 MHz d) 8 MHz. ☐

xii) The instruction cycle time to execute the instruction MOV A M is (clock frequency = 2 MHz)

a) 7 μs b) 1.5 μs

c) 3.5 μs d) 2 μs. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. What is the difference between. μ-processor & μ-controller ? What is the result of following codes & where is it kept ?

```
MOV  R4, # 25H
MOV  A, # 1FH
ADD  A, R4
```

3. A set of eight readings is stored in memory starting from memory location 9100H. Write a program to arrange them in ascending order.

4. Draw the timing diagram of opcode fetch machine cycle. How does ALE demultiplex the address bus from multiplex bus ? 3 + 2

5. Differentiate between :

   a) I/O mapped I/O and Memory mapped I/O

   b) Partial decoding and absolute decoding techniques. 3 + 2

6. Setup the 8254 as a square wave generator with a 1m/s period, if the i/p freq. to the 8254 is 1MHz.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) What are the methods of converting an assembly language program into its corresponding machine code ?

   b) Specify the contents of accumulator, register B, carry and zero flag as the following instructions are executed :

A	B	CY	Z
XX	XX	X	X

```
MVI A, 01
DCR A
MOV B, A
DCR B
SUI 01
HLT
```

   c) Draw the timing diagram for the instruction 'INR M' stored in memory location 8500H. 2 + 6 + 7

8. a) What is memory interfacing ? Design a memory interfacing circuit of DRAM (1024X8) and specify the address range whose address will be started from C000H.

   b) Write an assembly language program in 8085 μP to differentiate positive and negative data from given ten data and store the result in separate memory locations.

   c) What is RIM and SIM ? Write their functions. 7 + 5 + 3

9. a) Describe different functional units of 8254 with a block schematic representation.

   b) Interface an octal buffer as an input port and an octal latch as an output port with 8085. Connect 8 switches with the buffer and 8 LEDs in common anode configuration with the latch. The switch when closed should input a '1' to the 8085. Write a program to read the switch status and display it on the 8 LEDs. Also calculate the number of closed switches and store it reg. B. Consider the address of buffer to be 84H and that of latch to be 48H. 6 + 9

10. a) What is Programmable interrupt Controller ? Discuss with block diagram.

    b) What is ICW and OCW ?

    c) Specify the bit of a control word for the 8255, which differentiates the I/O mode and BSR mode.

    d) What do you mean by PUSH PSW ? 7 + 3 + 3 + 2

11. Write short notes on any three of the following : 3 × 5

    a) Programmable interval timer (PIT)

    b) RS 232 C standard

    c) Serial operation using 8085 μp

    d) 8257 DMA controller.

END