Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech(EIE-NEW)/SEM-4/EI-402/2013

2013

MICROPROCESSORS AND COMPUTER ARCHITECTURE

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

i) Which are the software interrupts in 8085μP ?

a) RST 0-7

b) RST 5.5 – 7.5

c) INTR

d) TRAP.

ii) When the IN and OUT instructions are executed, the address of I/O device is placed in low order address bus. At this time, the high order address bus content will be

a) 00H

b) Don't care

c) FFH

d) Same content as of low order address bus.

iii) SIMD stands for

a) Source index multiple data

b) Stack increment multiple data

c) Subtraction index multiple data

d) Single instruction stream, multiple data stream.

iv) The memory map of a 8 kB memory chip begins at the location E000H. The last location of the memory address and number of pages in the chip are

a) EF00H, 2

b) F000H, 8

c) FFFFH, 32

d) E000H, 16.

v) Machine cycle in "INRM" instruction are

a) 6

b) 5

c) 4

d) 3.

vi) The port of 8255 which can be used in BSR mode is

a) Port A only

b) Port B only

c) Port C only

d) Port D only.

vii) PSW is a

a) 16 bit register

b) 32 bit register

c) 08 bit register

d) 06 bit register.

viii) Associative memory is a

a) very cheap memory

b) pointer addressable

c) content addressable memory

d) slow memory.

ix) Cache memory

a) increases performance

b) increases machine cycle

c) reduces performance

d) none of these.

x) INR instruction affects

a) all flags

b) all flags exept zero flag

c) all flags except carry flag

d) no flags.

xi) 8085 microprocessor is an example of

a) Harvard architecture

b) Von Neumann architecture

c) Both (a) & (b)

d) None of these.

xii) How many T-states are required to execute DAD B instruction ?

a) 10

b) 13

c) 4

d) 6.

xiii) SIM instruction is used to

a) enable RST 7.5, 6.5, 5.5

b) disable RST 7.5, 6.5, 5.5

c) enable or disable RST 7.5, 6.5, 5.5

d) enable INTR.

xiv) What will be the content of PC after execution of the last instruction in the following program ?

B 12B : LXIH, 9100H

MOV A,M

INR L

ADDM

a) B130H

b) B12FH

c) B131H

d) B230H.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. What is speed up ratio of pipeline processing ?

   A non-pipeline system takes 50 ns to process a task. The same task can be processed in a six segment pipeline with a clock cycle of 10 ns. Determine the speed up rato of the pipeline for 100 tasks. What is the maximum speed up that can be achieved ? 1 + 4

3. Draw the timing diagram of DCR M instruction.

4. In Mode l configuration of 8255 P.P.I., what are the handshaking signals when Ports *A* & *B* act as output ports ? Briefly discuss their functions. 1 + 4

5. Define addressing mode. Briefly discuss different addressing modes for 8085 μP with suitable examples. 1 + 4

6. Mention the different modes of operation of 8254 PIT. Explain Square wave generator Mode of 8254 PIT. 2 + 3

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Draw the architecture of 8085 microprocessor.

   b) How does a microprocessor differentiate between data and instruction code ?

   c) What are the functions of "Program Counter" and "Stack Pointer" ?

   d) State what happens to the Flag register when the instruction SUB B and CMP B are executed in Intel 8085. 5 + 3 + 4 + 3

8. a) Define instruction cycle and machine cycle.

   b) Specify the contents of resister *A* and *B* and the status of flags *S*, *Z* and *CY* as the following instructions are executed.

   XRA A

   MVI B, 4AH

   SUI 4FH

   ANA B

   HLT

   c) Explain about the following instructions of 8085

      i) DAD D

      ii) XCHG

      iii) DAA

      iv) PCHL.

   d) Name the pins available in Intel 8085 for serial data communication. 2 + 3 + 8 + 2

9. a) Interface the following memory devices accroding to the given address map.

Memory	Capacity	Starting address
RAM	4 kB	9000_H
EPROM	2 kB	4000_H
EPROM	4 kB	6000_H

Will this system work ? If not, suggest changes in the address map to make it functional. 8 + 2

b) Write a program for the addition of 8 BCD numbers stored in consectutive memory locations starting from 9000_H. Store the result from 9100_H. 5

10. a) What do you mean by maskable and non-maskable interrupts of 8085 ? Write a program to check whether RST 6.5 is pending. If it is pending, enable it without affecting the masking status of the other interrupts. 2 + 4

b) Explain mode 2 operation of 8254. 3

c) With the help of a block diagram explain the operation of keyboard/display controller 8279. 6

11. Write short notes on any *three* of the following : 3 × 5

a) Asynchronous mode of data transfer

b) Von-Neumann bottleneck

c) I/O mode of 8255 PPI

d) Bus Idle machine cycle

e) Characteristics of multiprocessors.