Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech(EE/NEW)/SEM-6/EE-605C/2013

2013

VLSI AND MICROELECTRONICS

Time Allotted : 3 Hours *Full Marks :* 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) VLSI stands for

a) Very Large Scale Integration

b) Very Low Scale Integration

c) all of these

d) none of these.

ii) In LSI maximum number of transistors per chip is

a) 10000 b) 1000

c) 2000 d) none of these.

iii) ASIC stands for

a) Application Surface Integral Circuit

b) Application Specific Integral Chip

c) Application Specific Integrated Circuit

d) All of these.

iv) FPGA is used for

a) design verification b) front end design

c) design configuration d) none of these.

v) PLA stands for

a) Programmable Logic Array

b) Portable Logic Array

c) Programmable Linear Array

d) all of these.

vi) E-mos is normally

a) On device b) Off device

c) Can't be said d) all false.

vii) CMOS inverter requires minimum

a) 2 transistors b) 4 transistors

c) all of these d) none of these.

viii) VHDL is a

a) language b) hardware

c) PLA d) none of these.

ix) 2-input OR gate requires

a) 2 transistors b) 5 trnsistors

c) 1 ransistor d) 4 transistors.

x) D-MOSFET means

a) Depletion MOSFET b) Direct MOSFET

c) all of these d) none of these.

xi) Charge inversion can be observed in

a) BJT b) E-MOS

c) Diode d) all of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Draw NOR and NAND gates using CMOS. $2 \times 2\frac{1}{2}$

3. Write the advantages of VLSI technology.

4. Sketch $Y = \overline{(A + B + C).D}$

5. Sketch a stick diagram of 3-input NAND gate.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

6. a) Draw an inverter circuit using CMOS.

   b) Design a circuit using PAL to implement the following function :

   $F_1 = xyz + x^{/}y^{/}$

   $F_2 = w^{/}F_1^{/} + wxy^{/}z$

   c) Write a short note on FPGA. 3 + 7 + 5

7. a) Write a short note on y-chart.

   b) Sketch a stick diagram of $Y = \overline{(A + B + C).D}$.

   c) Describe working principle of Enhancement MOSFET.

   5 + 5 + 5

8. a) Write a VHDL programme for Full Adder.

   b) Write a VHDL program for X-OR gate.

   c) Write a short note on photo-lithography. 5 + 5 + 5

9. Write short notes on any *three* of the following : 3×5

   a) PLA

   b) Ion-implantation

   c) ASIC

   d) Depletion MOSFET.