MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : EC(EE)-302

DIGITAL ELECTRONIC CIRCUITS

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) A ring counter is
   a) shift register b) synchronous counter
   c) up-down counter d) none of these.

ii) Number of flip-flop required for a mod 15 ripple counter is
   a) 3 b) 4
   c) 5 d) 6.

iii) In AND-OR relation is equivalent to
   a) SOP b) POS
   c) K-map d) none of these.

iv) The equivalent octal number of hexadecimal number $AB2_{16}$ is
   a) 6272_8 b) 5262_8
   c) 5268_8 d) 2562_8.

v) The output of a two input NAND gate is HIGH if
   a) both inputs are LOW
   b) one of the input is HIGH and the other one is LOW
   c) both inputs are HIGH
   d) none of these.

vi) A 4 bit serial adder requires
   a) a half adder b) 4 half adder
   c) 4 full adder d) a full adder.

vii) All Boolean expressions can be implemented with
   a) AND gates only
   b) NOR gates only
   c) Combination of AND and OR gates
   d) None of these.

viii) D/A conversion will use an input as
   a) hexadecimal number
   b) an octal number
   c) a binary number
   d) analog wave.

ix) Which of the following devices allows only one output to be activated at one time ?
   a) Multiplexer
   b) Demultiplexer/decoder
   c) Encoder
   d) None of these.

x) The main advantage of Schottly TTL logic family is its least
   a) Power dissipation
   b) Propagation delay
   c) Fan-in
   d) Noise immunity.

xi) The fastest logic is
   a) TTL b) ECL
   c) IIL d) RTL.

xii) Asynchronous counter differs from a synchronous counter in
   a) the mod number
   b) the method of clocking
   c) the type of flip-flop used
   d) the number of states in a sequence.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. Explain race around condition of *J-K* flip-flop. Show how this condition can be avoided. 3 + 2
3. What is a BCD code ? What are its advantages and disadvantages ? 2 + 3
4. Design a 5 : 32 decoder using 3 : 8 decoder and 2 : 4 decoder.
5. Write short notes on weighted and non-weighted codes.
6. Briefly describe Johnson counter with proper diagram.

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GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. What is ripple counter ? Design a presettable 4-Bit up asynchronous counter using *J-K F-F*. A binary ripple counter is required to count to $(16383)_{10}$. How many *F-Fs* are required ? If the clock frequency is 8·192 MHz, what is the frequency at the output of the MSB ? 2 + 7 + 6
8. a) Design MOD 10 asynchronous Up/Down counter with *JK* flip-flop.
   b) Write down the difference between combinational circuit and sequential circuit. 12 + 3
9. a) Using *k*-map method, simplify the following function :
   $F(w, x, y, z) = \sum(1, 3, 4, 5, 6, 7, 9, 12, 13)$.
   b) What do you mean by SOP and POS ?
   c) What do you mean by Maxterm and Minterm ?
   d) State DeMorgan's theorem. 6 + 4 + 2 + 3
10. a) Design the following function using suitable MUX : *h* :
   $F(A, B, C, D) = \sum(1, 3, 4, 11, 12, 13, 14, 15)$
   b) Design a 16 : 1 MUX using 4 : 1 MUX.
   c) Design full substractor using two half substractor. 5 + 5 + 5
11. Write short notes on any *three* of the following : 3 × 5
   a) Even parity generator and checker
   b) R-2R ladder type DA converter
   c) EEPROM
   d) PLD
   e) TTL.