Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.TECH (ECE) (Separate Supple)/SEM-7/EC-702/2011

2011
EDA FOR VLSI DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable.

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) The logic family which consumes least amount of power is

   a) RCTL b) CMOS

   c) TTL d) none of these

   ii) Currently ASICs have a maximum gate count of about

   a) 500 000 b) 20 000

   c) 50 000 d) none of these.

   iii) MPGA is an acronym of

   a) Mask-Programmable Gate Array

   b) Minimum Position of Gate Array

   c) Maximum Position of Gate Array

   d) Most-Programmable Gate Array.

iv) The ASIC function is precisely defined in term of :

a) FPGA

b) PAL

c) MPGA

d) TTL/CMOS SSI and MSI

v) A PLA can be used

a) as a microprocessor

b) as a dynamic memory

c) to realise a sequential logic

d) to realise a combinational logic.

vi) The basic length unit λ is about a few

a) μm b) nm

c) μs d) m.

vii) TTL has the following advantage over CMOS

a) lower P_D

b) use of transistors alone as circuit element

c) greater suitability for LSI

d) simpler fabrication process.

viii) Half-Adder is also known as

a) AND circuit b) NAND circuit

c) NOR circuit d) EX-OR circuit.

ix) A hardware abstraction of the digital system is called

a) architecture body b) entity

c) package body d) none of these.

x) EDA stands for

a) Electronic Design Automation

b) Electrical Design Automation

c) Entity Declaration for Array

d) Electronic Digital to Analog Converter.

xi) Very Large Scale Integration (VLSI)

a) refers to a small computer on a chip

b) cannot be applied to MOS types

c) refers to IC's with complexity below 100 gates

d) does not require costly process facilities.

xii) VHDL has been structured to describe hardware for

a) design b) simulation

c) testing d) documentation

e) All of these.

xiii) VHDL is formulated in terms of entity and

a) component declaration

b) component instantiation

c) package declaration

d) architecture declaration.

xiv) Example of a package is

a) std_logic

b) std_logic_1164

c) std_ulogic_std_logic_vector

d) std_ulogic_vector.

xv) The full form of the DRC is

a) Design Rule Check

b) Data Rule Check

c) Direct Routing Control

d) None of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. a) What are the advantages of VLSI ? 1

b) Why do we use the EDA tools for VLSI design ? 2

c) What is the LUT ? 2

3. a) Sketch a transistor level schematic for a CMOS 2-input XOR gate.

You may assume you have both true and complementary version of the inputs available. 2

b) Compare Micron layout design rule with Lamda based design rule. 3

4. Briefly discuss the ASIC categories and represent it in the block form. 5

5. a) What is VHDL ? 2

b) Show that the VHDL language can be regarded as an integrated amalgamation. 3

6. Write down VHDL code for full-substractor using the data flow approach and draw the circuit with truth table. 3+1+1

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Deduce the equations of current of an ideal NMOS transistor. 6

b) What is body effect ? 2

c) Give the flow diagram for the production of a mask layout design. 2

d) Sketch stick diagram for CMOS 3-input NAND gate and estimate the cell width and height. 5

8. a) What is the design unit ? 2

b) Is mixed style modelling allowed in VHDL ?

If yes, explain with an example. 1 + 4

c) Write down the difference between concurrent signal assignment statement and sequential signal assignment statement. 3

d) What is delta delay ? Give an example 2 + 3

9. a) Write down the PAL characteristics. 5

b) Give the flow diagram for the PLD design flow. 3

c) Give the flow diagram for the ASIC design. 3

d) What is the advantage of ASIC ? What is the disadvantage of FPGA ? 2 + 2

10. a) What is the main feature of VHDL ? 3

b) What is the VHDL library ? 2

c) Write down VHDL code for Octal-to-Binary Encoder. 5

d) Write down VHDL code for clocked RS flip-flop and draw the waveform. 5

11. Write short notes on any three of the following : 3 × 5

a) Simulation of Digital circuits using CAD tools

b) CPLD

c) Placement and routing

d) Process statement

e) PLA