Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech(ECE)/SEM-7/EC-702/2011-12

2011

EDA FOR VLSI DESIGN

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

   i) EDA tools are used by

      a) Logic circuit designers

      b) Chip designers

      c) Device designers

      d) Fabrication designers.

   ii) Which of the following design styles has the maximum design cost and performance ?

      a) FPGA b) Full custom

      c) Standard cell d) Gate array.

iii) Which technology is not used in FPGA ?

a) Static RAM technology

b) Dynamic RAM technology

c) Anti-fuse technology

d) E^2 PROM technology.

iv) In which type of ASIC, the cell size is variable ?

a) Full custom b) Standard cell

c) Gate array d) FPGA.

v) In the λ design rule the width of the well is in unit

a) 9 b) 12

c) 10 d) 6.

vi) Min-cut algorithm is a

a) placement algorithm

b) routing algorithm

c) testing algorithm

d) floor planning algorithm.

vii) Which one is true for a Dataflow graph ?

a) Directed and acyclic

b) Directed and cyclic

c) Directed and can be both cyclic and acyclic

d) Undirected and acyclic.

viii) High level synthesis has design constraints like

a) area b) timing

c) power d) all of these.

ix) With T-SPICE, we can

a) perform fast, accurate simulations for analog and mixed signal IC designs

b) reduce run times to a great extent

c) gain simulation control and edit input circuit descriptions

d) all of these.

x) In constant field scaling which parameter is not scaled down ?

a) Device dimension

b) Doping concentration

c) Drain to source voltage

d) Aspect ratio (W/L) of the device.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. What is ASIC ? What are the steps in ASIC design flow ?

3. Distinguish between CPLD and FPGA.

4. Why do we prefer SRAM in FPGA ? Write the advantages and limitations of such use.

5. Write VHDL code in behavioural mode for a full adder.

6. What do you mean by testability of a circuit ? Give a comparison between different combinational test technologies.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Explain layout and physical design in VLSI circuit design.
   b) What do you mean by stick diagram ? Draw the stick diagram for CMOS inverter.
   c) What is logic synthesis ? What are the optimization techniques involved with this ? 4 + 6 + 5
8. a) What are the different styles of describing the architecture in VHDL ? Explain with example.
   b) Write down the VHDL code for 4 to 1 MUX and obtain the code for 16 to 1 MUX using this 4 to 1 MUX module. 9 + 6
9. a) What is the Min-cut algorithm ? Describe the different types of Min-cut algorithm.
   b) Describe the Kernighan-Lin algorithm for partitioning with a suitable example.
   c) What is SIA road map ? What are the design issues in DSM level ? 6 + 5 + 4
10. a) Why do we need CAD tools ? Explain.
    b) How do we check the functionality of our VHDL program using verification by simulation and verification using common test bench.
    c) Explain the difference between entity and architecture in a VHDL program.
11. Write short notes on any *three* of the following : 3 × 5
    a) Dataflow graph
    b) PLA and PLD
    c) Scan based technique
    d) Analog design automation
    e) RTL
    f) Static timing analysis.