Name : ....

Roll No. : ....

Invigilator's Signature : ....

CS/B.Tech(ECE)/SEM-5/EC-503/2009-10

2009

COMPUTER ARCHITECTURE & ORGANISATIONS

Time Allotted : 3 Hours   Full Marks : 70

The figures in the margin indicate full marks.

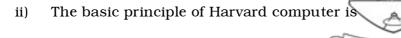*Candidates are required to give their answers in their own words as far as practicable.*

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following :

$10 \times 1 = 10$

i) A digital computer has a common bus system for 16 registers of 32-bits each. How many MUX are needed and what will be the size of each MUX ?

a) 32, 16

b) 16, 32

c) 8, 16

d) 16, 8.

55704   [Turn over

ii) The basic principle of Harvard computer is

a) storing program and data in separate memory

b) storing program and data in same memory

c) using pipeline concept

d) using a large number of registers.

iii) A digital computer has a memory unit of 32 k ∞ 12 k and cache memory of 512 ∞ 12 words. The cache uses direct mapping. How many bits are there in tag, index field ?
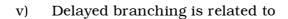
a) 6, 10   b) 10, 6

c) 9,6   d) 6, 9.

iv) A 'hit' occurs

a) when word is found in virtual memory

b) when word is found in cache memory

c) when word is not found in virtual memory
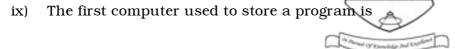
d) when word is not found is cache memory.

v) Delayed branching is related to

   a) Pipeline hazard   b) Pipeline remedy

   c) both (a) & (b)   d) none of these.

vi) Normilized representation of $0\cdot00101 \propto 2^2$ is

   a) $0\cdot00101 \propto 2^2$ b) $1\cdot01 \propto 2^2$

   c) $1\cdot01 \propto 2^{-1}$ d) none of these.

vii) Delayed branching is related to

   a) Pipeline hazard

   b) Pipeline remedy

   c) Both (a) and (b)

   d) none of these.

viii) Principle of Locality justifies the use of

   a) DMAb)   Cache Memory

   c) Main memory   d) none of these.

ix) The first computer used to store a program is

    a)   EDSAC   b)   ENIAC

    c)   EDVAC   d)   none of these.

x) Number of transistors in a CMOS static RAM cell is

    a)   1   b)   4

    c)   6   d)   none of these.

GROUP – B
(Short Answer Type Questions)
Answer any *three* of the following. $3 \infty 5 = 15$

2. Draw the control circuit for following RTL. :

$T_1 : A \longleftarrow B$

$T_2 : A \longleftarrow C$ 5

3. With diagram, distinguish between DRAM and SRAM.   5

4. a) Write key features of von Neumann architecture of a computer and mention the bottlenecks.

    b) How does Harvard architecture differ from von Neumann architecture ?   2 + 1 + 2

5. a) What is cache mapping ? Explain the difference between full associative and direct cache mapping.

1 + 2

b) What are 'write through' and 'write back' policies in cache ? 2

6. What are the different types of interrupt ? Give example. What is programmed I/O technique ? 5
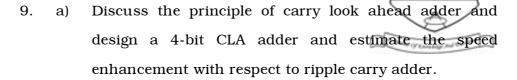
GROUP – C
(Long Answer Type Questions)
Answer any *three* of the following. $3 \times 15 = 45$

7. a) Using Booth's algorithm multiply (– 9) and (– 3), when numbers are represented in 2's complement form. 9

b) Show how non-restoring method is deduced from restoring division method. 4

c) Write down the steps of the algorithm of addition or subtraction of two floating point numbers. 2

8. a) Define MIMD type parallel processing. Define speed-up of a parallel processing system. 2 + 2

b) Show that when K jobs are processed over an N stage pipeline, the speed-up obtained is

$$Sp = (NK) / (N + K - 1)$$ 6

c) With the help of a neat diagram show the structure of a typical arithmetic pipeline performing $A * B + C$. 5

9. a) Discuss the principle of carry look ahead adder and design a 4-bit CLA adder and estimate the speed enhancement with respect to ripple carry adder.
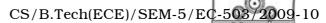
b) Briefly state the relative advantages and disadvantages of parallel adder over serial adder.

c) $X = (A + B) X C$

Write down the zero address, one address and three addresses instruction for the expression.

$(4 + 3) + 2 + 6$

10. a) Why DMA based I/O is better than other I/O techniques ? 3

b) Differentiate between isolated I/O and memory mapped I/O. 3

c) Explain DMA based data transfer operation between memory and other peripherals. 6

d) What is the difference between vectored and non-vectored interrupt ? 3

11. Write short notes any *three* of the following :   3 ∞ 5

    a)   Magnetic recording

    b)   Adder-subtractor circuit

    c)   Stack organization

    d)   Bus organization using tri-state buffer

    e)   DMA

    f)   Addressing modes.

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