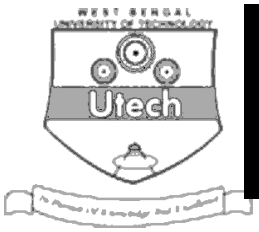
DIGITAL ELECTRONICS & INTEGRATED CIRCUITS
(SEMESTER - 4)

CS/B.Tech(ICE, EEE, EE(O), ECE(O), EIE(O), PWE)/SEM-4/EC-402/09



1. .....
Signature of Invigilator

2. .....
Signature of the Officer-in-Charge

Reg. No.

Roll No. of the Candidate

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CS/B.Tech(ICE, EEE, EE(O), ECE(O), EIE(O), PWE)/SEM-4/EC-402/09

ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2009

DIGITAL ELECTRONICS & INTEGRATED CIRCUIT (SEMESTER - 4)

Time : 3 Hours] [Full Marks : 70

INSTRUCTIONS TO THE CANDIDATES :

1. This Booklet is a Question-cum-Answer Booklet. The Booklet consists of **32 pages**. The questions of this concerned subject commence from Page No. 3.
2. a) In **Group – A**, Questions are of Multiple Choice type. You have to write the correct choice in the box provided **against each question**.
   b) For **Groups – B** & **C** you have to answer the questions in the space provided marked 'Answer Sheet'. Questions of **Group – B** are Short answer type. Questions of **Group – C** are Long answer type. Write on both sides of the paper.
3. **Fill in your Roll No. in the box** provided as in your Admit Card before answering the questions.
4. Read the instructions given inside carefully before answering.
5. You should not forget to write the corresponding question numbers while answering.
6. Do not write your name or put any special mark in the booklet that may disclose your identity, which will render you liable to disqualification. Any candidate found copying will be subject to Disciplinary Action under the relevant rules.
7. **Use of Mobile Phone and Programmable Calculator is totally prohibited in the examination hall.**
8. You should return the booklet to the invigilator at the end of the examination and should not take any page of this booklet with you outside the examination hall, **which will lead to disqualification**.
9. Rough work, if necessary is to be done in this booklet only and cross it through.

No additional sheets are to be used and no loose paper will be provided

FOR OFFICE USE / EVALUATION ONLY

Marks Obtained

	Group – A										Group – B				Group – C				
Question Number																		***Total Marks***	***Examiner's Signature***
Marks Obtained																			

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Head-Examiner/Co-Ordinator/Scrutineer

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GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) Which of the following is a reflected code ?

a) 8421 code b) Excess-3 code

c) Gray code d) ASCII code. ☐

ii) The value of base X for which $(211)_X = (0{\cdot}52)_8$ is

a) 08 b) 10

c) 16 d) 07. ☐

iii) Gray code of a number is 10110. What is its decimal number ?

a) 10 b) 15

c) 27 d) 25 ☐

iv) $(15)_{10} - (10)_{10}$ is equal to (using 1s complement)

a) 0101 b) 1010

c) 1110 d) 0010. ☐

v) If you want to convert a J-K FF to a D-FF then which gate is connected between J & K terminals of the J-K FF ?

a) AND b) OR

c) NOT d) EX-OR. ☐

vi) Conversion of $(110101.101010)_2$ to octal is

a) 65.52_8 b) 45.52_8

c) 55.52_8 d) 75.52_8

vii) Conversion of the Gray code 1101 to binary is

a) 1001 b) 1100

c) 0101 d) none of these.

viii) BCD coding of 12 is

a) 00001010 b) 00001100

c) 00010010 d) none of these.

ix) The result of the BCD addition of 00000111 & 00000011 is

a) 00001010 b) 00010000

c) 01000001 d) none of these.

x) Which gates are used as an array of a programme in ROM ?

a) AND gates b) OR gates

c) Both AND and OR gates d) None of these.

xi) The decimal equivalent of $(50)_7$ is

a) 03 b) 05

c) 07 d) 09.

xii) Which one of the following is known as associative law if X, Y and Z are three binary variables ?

a) $X + Y + Y + X$ b) $X (Y + Z) = XY + XZ$

c) $X + (Y + Z) = (X + Y) + Z$ d) $X + XY + X$.

xiii) For a shaft encoder, the most appropriate 2-bit code is

a) 11, 10, 01, 00 b) 11, 10, 00, 01

c) 01, 10, 11, 00 d) 01, 00, 11, 10. ☐

xiv) When J & K inputs are connected together of a J-K flip-flop then it becomes

a) D flip-flop b) T flip-flop

c) S-R flip-flop d) None of these. ☐

xv) R-2R ladder network is used as a/an

a) A/D converter b) AC to DC converter

c) BCD to Excss-3 converter d) D/A converter. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. Implement the following function using 4·1 multiplexers and other necessary logic gates. Connect *C* & *D* as select lines of the multiplexer.

$F(A, B, C, D) = \sum (0, 3, 10, 11, 12, 13, 15)$

3. Explain the circuit operation of a Master-Slave JK flip-flop using all NAND gates. Write down the corresponding truth table.

4. Design a 4 to 16 decoder by using two 3 to 8 decoders. Write down the corresponding truth table.

5. What is race around condition ? How can we overcome the race around condition ?

6. a) Why do we perfer to use Gray code in K-map ?

b) We can design *T* flip-flop using only a J-K FF. Can we do the same using S-R FF ? If yes, explain and if not, explain according to your answer.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Simplify the Boolean function :

$$F = \sum_{m}(0, 2, 3, 6, 7) + \sum_{d}(8, 10, 11, 15)$$ using *K*-map method.

b) Design a full-subtractor circuit with the help of full-adder circuit and one NOT gate. Write down the expression and truth table in favour of your design.

c) Which code is known as self complementing code ? Explain your answer. 7 + 5 + 3

8. a) Explain the operation of dual slope integration type A/D converter. Derive the expression of the output voltage.

b) Draw the circuit diagram of a 2 input TTL NAND gate and explain how it works. Write down the truth table.

c) What do you mean by resolution ? 7 + 7 + 1

9. Use a decoder of suitable size and other necessary logic gates to design a multiplier to multiply two 2-bit binary numbers $a_1\ a_0$ and $b_1\ b_0$ where a_0, a_1, b_0 and b_1 are the binary bits. Assume that the decoder has all active low outputs and one active low enable line. 15

10. a) What are the facilities available in universal shift register ? How a 4-bit universal shift register can be realized using multiplexers and flip-flops ?

b) Write down the count sequence of a 3-bit binary Down Counter. Design a Ripple counter using negative edge triggered *T* flip-flops for the sequence.

c) How can this counter be converted to a MOD-5 down counter ? 7 + 5 + 3

11. Write short notes on any *three* of the following : 3 ∞ 5

a) Johnson Counter

b) Propagation Delay

c) Parallel In Serial Out (PISO)

d) Even Parity Generator and Checker

e) 4-bit binary parallel adder.

END