



**MAULANA ABUL KALAM AZAD UNIVERSITY OF
TECHNOLOGY, WEST BENGAL**

Paper Code :EC(EI)-301

DIGITAL ELECTRONIC CIRCUITS

Time Allotted:3 Hours

Full Marks: 70

*The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words
as far as practicable.*

Group - A

(Multiple Choice Type Questions)

1. Answer any ten questions: <http://www.makaut.com> 1×10=10

(i) The minimum number of NAND gate required to design a single XOR gate is

- ✓ (a) 5 (b) 3
 (c) 4 (d) 6

(ii) The logic family which gives the fastest switching speed is

- ✓ (a) ECL (b) Schottky TTL
 (c) CMOS (d) Low Power Schottky TTL

(iii) $Y = AB + \bar{A}B + A\bar{B}$

- (a) All are minterms (b) The function is in canonical form
 ✓ (c) Both are true (d) None of them

(iv) The following operation is equivalent to <http://www.makaut.com>



- (a) A buffer or delayed gate (b) An inverter
 (c) Adder (d) None of them

Turn Over

(vi) 10MHz clock signal is applied to a MOD-4 counter followed by a MOD-5 counter then the output clock frequency will be

- (a) 50 kHz (b) 5 MHz
(c) 5 kHz (d) 500 kHz

0111 1001 0011

(vii) BCD equivalent of $(293)_{10}$ is <http://www.makaut.com>

- (a) 0111 1001 0011 (b) 1011 1001 0011
(c) 0111 1001 0101 (d) 0111 1010 0011

(viii) If $(511)_x = (777)_8$ then the value of x is

- (a) 6 (b) 7
(c) 5 (d) 3

(ix) A single bit memory device is

- (a) ROM (b) RAM
(c) FLIP-FLOP (d) PROM

(x) The operation of a flip-flop is analogous to

- (a) Astable multivibrator (b) Monostable multivibrator
(c) Bistable multivibrator (d) None of these

(xi) For a N-bit weighted register D/A converter number of resistors required is

- (a) 2N (b) N
(c) 2N-1 (d) N-1

(xii) The minterms for $F(A,B,C) = A + \overline{BC} + BC$ are <http://www.makaut.com>

- (a) $\sum m(0,1,2,3,4,6)$ (b) $\sum m(0,3,4,5,6,7)$
(c) $\sum m(1,3,4,5,6,7)$ (d) $\sum m(0,2,3,4,5,7)$

(xiii) A ring counter consists of 6 flip-flops will have

- (a) 12 states (b) 6 states
(c) 11 states (d) 5 states

Group - B

(Short Answer Type Questions)

Answer any three of the following.

5×3=15

1. Using the theorem of Boolean logic prove that

$$(A + B).(\overline{A\overline{B}} + C).(\overline{A\overline{C}} + \overline{B}) = \overline{A}B + B\overline{C}$$

2. Simplify $F(A,B,C,D) = \sum m(1,3,7,11,15) + \sum M(0,2,5)$ using k-map and realize the simplified expression using NAND gates only 2+2+1=5

3. Design a 4 bit adder/subtractor module using full adder and necessary gates with an add/subtract control line.

4. Implement the function $F(A,B,C,D) = \sum m(1,2,3,7,8,9,11,15)$ using a single 8-1 MUX considering A,B,D as a select lines.

5. Design a 4 bit universal shift register using 4-1 MUX and other gates. <http://www.makaut.com>

Group - C

(Long Answer Type Questions)

Answer any three of the following.

15×3=45

7. Find the minimal expression for the function $F(A,B,C,D) = \sum m(1,3,4,5,9,10,11) + \sum d(6,8)$ using Quine McClusky method and also realize the expression using only two input basic logic gates. 12+3=15

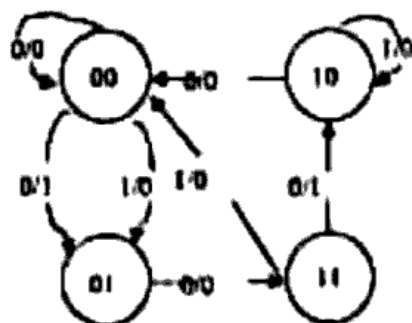
8. (a) What did you mean by Race around condition? How it can be eliminated using Master Slave flip-flop?

(b) Realize a T flip-flop using SR flip-flop.

(c) How do you cascade two 2-4 decoders to make one 3-8 decoder? Draw the necessary circuit.

(2+4)+6+3=15

9. (a) Design a clocked synchronous sequential network using J-K flip-flop and other gates whose state diagram is given below. <http://www.makaut.com>



(b) Design a mod-5 ripple counter using J-K flip-flop.

10×5=15

CS/B.Tech/EIE/Odd/SEM-3/EC(EI)-301/2018-19

10. (a) Explain the operation of a 4 bit R-2R ladder digital to analog converter.
(b) For the same circuit assume that the feedback resistance of the op amp is variable, the resistance $R=10K\text{-ohm}$ and reference voltage $V_R=10V$. Determine the value of R_f that should be connected to achieve the following output conditions:
- (i) The value of 1 LSB at the output is 0.5 V
 - (ii) An analog output of 6 V for a binary input of 1010.
 - (iii) The full scale output voltage of 12 V.
 - (iv) The actual maximum output voltage of 10 V. 7+8=15

11. Write short notes on *any three* of the following: <http://www.makaut.com> 5×3=15

- (i) Basic principle of successive approximation type A/D converter
 - (ii) Parity Generator
 - (iii) Johnson counter
 - (iv) Parallel in Serial Out Register
 - (v) EEROM
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