

CS/B.TECH/ECE/ODD SEM/SEM-7/EC-702/2016-17



**MAULANA ABUL KALAM AZAD UNIVERSITY OF
TECHNOLOGY, WEST BENGAL**

Paper Code : EC-702

MICROELECTRONICS & VLSI DESIGNS

Time Allotted : 3 Hours

Full Marks : 70

The figures in the margin indicate full marks.

*Candidates are required to give their answers in their own
words as far as practicable.*

GROUP - A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the
following : $10 \times 1 = 10$

i) In which device has the highest carrier mobility ?

a) NMOS

b) PMOS

☒ c) CMOS.

ii) Which device acts as good switch ?

a) NMOS

b) PMOS

☒ c) CMOS.

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iii) In which device at zero gate voltage the channel
already exist ?

☒ a) Depletion type MOSFET

b) CMOS device

c) Enhance type MOSFET.

iv) The condition, where the majority carrier
concentration is greater near the Si-SiO₂ interface
compared to the bulk in the MOSFET is called

☒ a) Accumulation

b) Depletion

☒ c) Inversion.

v) The potential at which the inversion layer
dominates the substrate behaviour is

a) Pinch-off voltage

b) Cut-off voltage

☒ c) Threshold voltage.

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vi) The overlap capacitance is

- ☒ a) voltage dependent
- b) voltage independent
- c) none of these.

vii) Which has highest noise margin ?

- a) active load inverter
- b) resistive load inverter
- ☒ c) CMOS inverter.

viii) Which is correct for the accumulation region ?

- a) $V_{GB} < V_{FB}$
- ☒ b) $V_{GB} > V_{FB}$
- c) $V_{GB} = V_{FB}$

ix) The static power dissipation is NIL for

- a) single transistor dynamic RAM
- b) Pseudo-static RAM
- ☒ c) Static RAM.

x) Which design is more efficient ?

- a) Pull up & Pull down design
- ☒ b) TG design
- c) Pre-charge & evaluate logic.

xi) Overlapping capacitance of MOS denotes

- a) capacitance between drain and oxide layer
- b) capacitance between source and oxide layer
- ☒ c) both (a) and (b).

GROUP - B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

☒ 2. Explain the following phenomena in a MOS structure :

- a) Channel length modulation
- b) Scaling of MOSFET. 2 + 3

☒ 3. a) Explain the working principle of a CMOS inverter.

- b) Draw the VTC curve of a simple CMOS inverter circuit and clearly define the different operating regions of NMOS and PMOS. 2 + 3

4. ✓ What is modularity and locality of VLSI design ?
5. Design a half subtractor circuit using PLA.
6. Design a PROM which takes 3 binary bits as input and generates the output which is the square of the input.

GROUP - C**(Long Answer Type Questions)**

Answer any *three* of the following. $3 \times 15 = 45$

7. a) What is "divide and conquer method" ? Explain.
- b) Draw the layout and schematic diagram of a 2-input static CMOS NAND gate and clearly identify the corresponding components in the two drawings.
- c) With suitable diagram briefly describe the p-well fabrication process of a CMOS inverter.
- d) What is micron rule ? $2 + 5 + 6 + 2$

8. a) Design a CMOS half adder using smallest possible number of transistors.
- b) Draw a clocked *D* flip-flop using CMOS and explain.
- c) Design a transmission Gate based XNOR gate using six transistors.

d) What is pseudo-NMOS logic ? $6 + 4 + 3 + 2$

9. ✓ a) Distinguish between diffusion and ion-implantation technique.

b) What is photolithography ? Explain.

c) What is meant by Molecular Beam Epitaxy (MBE) ?

d) Explain how MOSFET can be used as resistor.

$4 + 5 + 3 + 3$

10. a) What is current mirror ? Explain with proper circuit diagram.
- b) Draw the block diagram of a two-stage op-amp and explain the function of each block.
- c) How can you realize the resistor using switched capacitor circuits ?
- d) What is switched capacitor filter ? $(1 + 3) + 5 + 4 + 2$

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11. Write short notes on any *three* of the following : 3 × 5

- ✓ a) FPGA
 - b) MOS capacitor
 - c) Programmable Logic Array
 - d) Ion Implantation
 - ✓ e) Czochralski technique for crystal growth
 - ✓ f) Y chart of VLSI design flow.
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