EC-702

MICROELECTRONICS AND VLSI DESIGNS

Time Allotted: 3 Hours | Full Marks: 70

The figures in the margin indicate full marks.
Candidates are required to give their answers in their own words as far as practicable

GROUP A
(Multiple Choice Type Questions)

1. Answer any *ten* questions. 10×1 = 10

(i) The output of physical design is

(A) Layout (B) Mask
(C) RTL (D) Circuit Design

(ii) A MOS device can be used as a resistor in

(A) linear region (B) saturation region
(C) sub-threshold condition (D) none of these

(iii) The unit of trans-conductance parameter of MOSFET is

(A) $\mu A^2/V^2$ (B) $\mu A/V^2$
(C) $\mu A^2/V$ (D) $\mu A/V$

(iv) The data refresh operation is needed in

(A) SRAM (B) DRAM
(C) EEPROM (D) FLASH

(v) Which DRAM i/p buffer has lowest power consumption and fastest in operation?

(A) inverter type buffer (B) latch-type buffer
(C) differential amplifier type buffer (D) both (B) and (C)

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(vi) The disadvantages of flash memory is

(A) high electrical voltage required to erase data
(B) total block of memory is erased at a time
(C) very slow writing speed

(vii) Among the following which one has the greatest gate integration capacity?

(A) FPGA (B) CPLD
(C) PLD (D) ASIC

(viii) FPGA is a

(A) full-custom ASIC (B) semi-custom ASIC
(C) programmable ASIC (D) none of these

(ix) VHDL is a

(A) multithreaded program
(B) a programming language like C
(C) single user program
(D) sequential program

(x) The body effect occur due to potential difference between

(A) source and body (B) body and drain
(C) gate and body (D) none of these

(xi) In channel length modulation, the drain current

(A) increase (B) decrease
(C) constant (D) zero

(xii) PMOS are wider than NMOS transistor

(A) mobility of holes is less than electrons
(B) mobility of holes is greater than electrons

GROUP B
(Short Answer Type Questions)

Answer any *three* questions. 3×5 = 15

2. What is current source and current sink in VLSI circuit? Design a current sink using $V_{DD} = -V_{SS} = 2.5$ V to sink a current of 10 μA. Estimate the minimum voltage across the current source and the output resistance. Assume $K_P = 50\ \mu A/V^2$, $L = 5\ \mu m$, $V_{THN} = 0.83$ V, $\lambda = 0.06$. 2+3

3. Draw and explain the operation of MOS Switched Capacitor Integrator and also find the expression for output voltage. 5

4. Design a half adder using standard CMOS AOI logic. If the Precharge-Evaluate (PE) logic is used to design the same circuit, how many transistors will be required? In the Industrial view, which technology is preferable? 2.5+1.5+1

5. Compare between static logic and dynamic logic. Explain the operation of Domino-logic to design any CMOS circuit. 2+3

6. What is Transmission Gate (TG)? Explain the operation of Edge Triggered D Flip-Flop using CMOS TG gates. Implement the expression using CMOS TG logic. Z = XY' + X'Y. (X' = complement of X) 1+2+2

GROUP C
(Long Answer Type Questions)

Answer any *three* questions. 3×15 = 45

7. (a) What is an ideal op-amp? 2

   (b) Draw the block diagram of two stage CMOS OPAMP. 3

   (c) Find the "Input common mode range" and "Output swing" of a two-stage CMOS OMP AMP. 5

   (d) In a two stage CMOS OPAMP is fabricate in a process for which $V'_{An} = |V'_{Ap}| = 20$ V/μm. Find A_1, A_2 and A_V if all devices are 1 μm long. $V_{ov1} = 0.2$ V and V0v6 = 0.5 V. Also find the OPAMP output resistance obtained when the 2nd stage is biased at 0.5 mA. 5

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8. What is lithography? Mention various types of lithography used in VLSI. What are the differences between PPR and NPR? What are prebake and postbake in lithography? What are the characteristics of exposure tools used in lithography?

9. Explain the following dominant CMOS fabrication process with neat diagrams. 4
   (a) P-well process
   (b) N-well process
   (c) Twin tub process
   (d) Silicon on insulator

10. What is oxidation? With a diagram, explain silicon thermal oxidation process. Determine the ratio of silicon consumed to the thickness of grown SiO_2 layer over the wafer. If a SiO_2 layer of 1200 Å is to be grown, what would be the thickness of used silicon? Given, molecular weight of SiO_2 = 61.09 g/mol, density of SiO_2 = 2.25 g/cc, atomic weight of Si = 28.12 g/mol, density of Si = 2.45 g/cc.

11. Write short notes on any *three* of the following
   (a) VLSI interconnects
   (b) Folded-cascode amplifier
   (c) LIGA process
   (d) Clean room
   (e) High K dielectric materials for IC fabrication.