Name : .....

Roll No. : .....

Invigilator's Signature : .....

CS/B.Tech (ECE-NEW)/SEM-6/EC-604/2010

2010

VLSI CIRCUITS AND SYSTEMS

Time Allotted : 3 Hours *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : 10 × 1 = 10

   i) Scaling is done for

      a) improving the switching speed

      b) reducing the power dissipation

      c) decreasing the chip size

      d) all of these.

   ii) For 0·25 μm process what is the value of λ ?

      a) 0·5 μm b) 0·125 μm

      c) 0·75 μm d) 1 μm.

iii) The two transitional critical points on the VTC curve are identified where the slope becomes

a) -1 b) $+1$

c) 0 d) ∞.

iv) Noise margin for low signal levels (NM_H) is

a) $V_{IL} - V_{OL}$ b) $V_{IH} - V_{IL}$

c) $V_{OH} - V_{IH}$ d) $V_{OH} - V_{IL}$.

v) The threshold voltage of an enhancement *n*MOS transistor is

a) greater than 0 V b) less than 0 V

c) equal to 0 V d) none of these.

vi) The (W/L) ratio of the *p*MOS and *n*MOS transistors for an ideal symmetric inverter is

a) 1 b) 3·5

c) 2·5 d) 4.

vii) The equivalent (W/L) of two *n*MOS transistors with (W_1/L) and (W_2/L) connected in parallel is

a) $(W_1/L)+(W_2/L)$ b) $(W_1/L).(W_2/L)$

c) $1/(L/W_1 + L/W_2)$ d) $(W_1/L)/(W_2/L)$.

viii) In MOSFET threshold voltage depends on

a) gate voltage b) source voltage

c) drain voltage d) all of these.

ix) In a short channel MOS structure electron mobility

a) increases

b) decreases

c) remains same

d) first increases then decreases.

x) CMOS inverter is useful because it has

a) low sensitivity to noise

b) low power consumption

c) excellent speed

d) all of these.

xi) The main advantage of precharge-evaluate dynamic logic is

a) lesser number of transistors required

b) high speed

c) low power consumption

d) all of these.

xii) When two *n*MOS are connected in parallel, the equivalent k_n is given by

a) $2k_n$ b) $k_n/2$

c) k_n d) none of these.

xiii) How many transistors are required to design the function $F=(ABC+DE)'$ using CMOS logic ?

a) 5 b) 7

c) 10 d) 14.

xiv) In the region C of the VTC curve of CMOS inverter

a) *p*MOS is linear & *n*MOS is in saturation

b) *p*MOS is in saturation & *n*MOS is in linear

c) *p*MOS is in saturation & *n*MOS is in saturation

d) *p*MOS is in linear & *n*MOS is in linear.

xv) A MOS device can be used as a resistor

a) in linear region b) in saturation region

c) sub-threshold region d) none of these.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) Explain the VLSI design flow with the help of Y-chart.

b) Discuss the concepts of regularity, modularity and locality in VLSI design. 3 + 2

3. Draw the VTC curve of a simple CMOS inverter circuit and clearly define the different operating regions of NMOS and PMOS.

4. Describe the following phenomena in MOS structure :

   a) I-V characteristics

   b) Channel length modulation.

5. a) What do you mean by CMOS Transmission Gate (TG).

   b) Design the following circuits using transmission gates : 2 + 3

      i) 2 input XOR gate

      ii) 2 × 1 MUX.

6. Explain with a circuit diagram, operation of a differential amplifier.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

7. a) Design a transmission gate full adder circuit and explain.

   b) What are the differences between PLA and PAL ?

   c) Implement the following two functions using PLA and PAL.

      i) $F1 = BA + C'B'A + CB'A'$

      ii) $F2 = C'B'A' + CBA$. 5 + 5 + 5

8. a) Where are the dynamic logic circuits preferred in comparison to static logic ?

   b) What is domino CMOS logic ? How the cascading problem in dynamic logic can be eliminated in domino logic ?

   c) What is the charge sharing problem in dynamic CMOS logic ? How can it be prevented ?

   d) Describe the operation of three transistor DRAM cell. 2 + 4 + 4 + 5

9. a) What are the differences in between diffusion and ion implantation ?

   b) Explain the fabrication steps of CMOS inverter with necessary diagrams. 3 + 12

10. a) Show that for a symmetric CMOS inverter the two noise margins are same and are equal to VIL. Also show that for ideal CMOS inverter $(W/L)_p = 2 \cdot 5 (W/L)_n$.

    b) What do you mean by design rules ? What are the differences in between lambda (λ) and micron (μ) rules. 10 + 5

11. Write short notes on any *three* of the following : 3 × 5

a) Constant voltage scaling

b) CMOS NORA logic

c) Drain Induced Barrier Lowering (DIBL)

d) CPLD

e) Dynamic RAM.