MAULANA ABUL KALAM AZAD UNIVERSITY OF TECHNOLOGY, WEST BENGAL

Paper Code : EC-402

DIGITAL ELECTRONICS AND INTEGRATED CIRCUITS

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) The 9's complement representation of $(3465)_{10}$ is

   a) 6534 b) 5346

   c) 4536 d) 3456.

   ii) Conversion of $(11011.101)_2$ to decimal number is

   a) 26·725 b) 27·625

   c) 25·675 d) 22·657.

   iii) A binary number with n bits all of which are 1s has the value

   a) $n^2 - 1$ b) 2^n

   c) $2^{(n-1)}$ d) $2^n - 1$.

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   iv) The Excess-3 code is a

   a) cyclic code

   b) weighted code

   c) self-complementing code

   d) error correcting code.

   v) What is the minimum number of two-input NAND gates used to perform the function of 2-input OR gate ?

   a) One b) Two

   c) Three d) Four.

   vi) The code used for labelling cells of the K-map is

   a) natural BCD b) Hexadecimal

   c) gray d) Octal.

   vii) The minimum number of 2-input NAND/NOR gates required to realize a half adder is

   a) 3 b) 5

   c) 4 d) 6.

   viii) The transparent Latch is

   a) S-R flip-flop b) D flip-flop

   c) T flip-flop d) J-K flip-flop.

   ix) In which type of ADC, the conversion time depends on the magnitude of the analog input

   a) counter-type

   b) flash-type

   c) successive-approximation type

   d) dual-slope type.

   x) The memory technology which needs the least power is

   a) ECL b) MOS

   c) CMOS d) none of these.

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xi) Race around condition is found in which flip-flop ?

a) D flip-flop b) J-K flip-flop

c) S-R flip-flop d) T flip-flop.

xii) The logic gate used in parity checker is

a) NAND gate b) NOR gate

c) X-NOR gate d) X-OR gate.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. What is race-around condition ? How is it overcome by using Master-slave J-K flip-flop ? Explain with logical diagram. 2 + 3

3. a) Differentiate between combinational logic circuit and sequential logic circuit.

   b) Minimize the following function Using K-Map method

   $F(A, B, C, D) = \sum_m (0, 2, 3, 6, 7) + \sum_d (8, 10, 11, 15)$

   and implement the circuit using basic gates. 2 + 3

4. Design a MOD 6 synchronous counter using J-K flip-flop and draw the timing diagram.

5. a) Implement full adder circuit using 3 : 8 decoder with additional logic gates.

   b) Design Binary to Gray code converter using logic gates. 3 + 2

6. Define the following parameters of DACs : 5×1

   a) Resolution

   b) Offset error

   c) Settling error

   d) Monotonicity

   e) Percentage resolution.

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. $3 \times 15 = 45$

7. a) Show how S-R flip flop can be converted into D flip-flop. 9

   b) Describe the operation of dual slope A/D converter with necessary diagram. 6

8. a) Design a Mod-6 asynchronous counter using T flip-flops. 6

   b) State the differences between asynchronous and synchronous counter. 3

   c) Design a synchronous counter with the following sequence : 6

   0000 — 0010 — 0100 — 0110 — 1000 — 1010 — 1010 — 1100 — 1110 — 0000 .....

9. a) What are the differences between LATCH and flip-flop ?

   b) Design a 2-bit ripple up-counter using J-K flip-flop and draw timing diagram.

   c) With a neat diagram describe how a shift register works as parallel-in serial-out mode. 2 + 4 + 9

10. a) Explain the operation of R-2R ladder type DAC with neat circuit diagram.

    b) Explain the working of a successive approximation register (SAR) type ADC. 7 + 8

11. Write short notes on any *three* of the following : 3×5

    a) Ring Counter

    b) Odd parity generator and checker

    c) Universal shift register

    d) Tri-state gates in TTL family

    e) Johnson counter.