ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE – 2008
DIGITAL ELECTRONICS & INTEGRATED CIRCUITS
SEMESTER – 4

Time : 3 Hours] [Full Marks : 70

GROUP – A
(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

i) The minimum number of NAND gates required to implement (A + AB′ + AB′ C′) is

a) zero b) one
c) four d) seven. ☐

ii) Conversion of $(36 \cdot 532)_8$ into equivalent hexadecimal number is

a) $(1F \cdot AE)_{16}$ b) $(1E \cdot AD)_{16}$
c) $(1F \cdot AD)_{16}$ d) None of these. ☐

iii) Conversion of $(564)_{10}$ into Gray code is

a) 1100101110 b) 1110100110
c) 0111001011 d) 1000110100. ☐

iv) If t_p is the pulse width, Δt is the propagation delay and T is the period of pulse train, then which one of the following conditions can avoid the race around conditions ?

a) $t_p = \Delta t = T$ b) $2t_p > \Delta t > T$
c) $t_p < \Delta t < T$ d) $2t_p < \Delta t < T$. ☐

v) The equation $\sqrt{213} = 13$ is valid for which one of the number systems with base ?

a) Base 8 b) Base 6
c) Base 5 d) Base 4. ☐

vi) Which one of the following is a self complementing code ?

a) Ex-3 code b) Gray code

c) 8421 code d) None of these. ☐

vii) A clock frequency of 100 kHz is applied to MOD – 8 followed by a decade counter. What will be the output frequency ?

a) 12·5 kHz b) 10 kHz

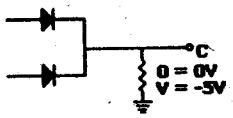
c) 1·25 kHz d) None of these. ☐

viii) A 3-bit synchronous counter uses flip-flops with propagation delay time of 20 ns each. The maximum possible time required for change of state will be

a) 60 ns b) 40 ns

c) 20 ns d) none of these. ☐

ix) If the negative logic is used, the diode gate shown in the given figure will represent



a) OR gate b) AND gate

c) NOR gate d) NAND gate. ☐

x) The minimum number of NAND gates required to implement $A+A\bar{B}+A\bar{B}C$ is equal to

a) 0 b) 1

c) 4 d) 7. ☐

xi) In standard TTL, the "totem pole" stage refers to the

a) multi-emitteer i/p stage b) phase splitter

c) o/p buffer d) open collector o/p stage. ☐

xii) The SOP form of logical expression is most suitable for designing logic circuits using only

a) XOR gates b) NOR gates

c) NAND gaes d) OR gates. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. What is fan out ? What is the basic difference of a latch and edge triggered flip-flop ?

Design a 9-bit even parity generator circuit. 1 + 1 + 3

3. Design BCD-Excess 3 code converter using basic logic gates with proper truth table. 5

4. What is Race Around condition ? Explain the working of Master-Slave Flip-flop. 1 + 4

5. Draw a neat diagram of a R-2R ladder type DAC and explain its operation. 5

6. Draw the neat diagram of a 4 bit Bi-directional Shift register using mode control (*M*).

When *M* is logic zero then left shift and right shift for *M* are logic one. 5

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following questions. 3 × 15 = 45

7. a) What do you mean by Prime implicant ? Simplify the following Boolean expression using K-map :

$F(A, B, C, D) = \Sigma m(0, 2, 3, 6, 8, 11, 12, 14) + d(1, 4, 9, 10)$

b) Design full adder using two half adders and necessary gate.

c) Draw a network using only NAND gate to generate the function $Y = (\overline{A} + BC)$.

(2 + 5) + 4 + 4

8. a) What are the advantage and disadvantage of totem pole ?

b) What are the output voltages caused by logic 1 in each bit position in an 8 bit ladder if the input level for 0 level is 0 volt and for level 1 is 10 volt ?

c) Compare the maximum conversion period of an 8 bit Digital ramp ADC and 8 bit successive approximation ADC if both utilize 1 MHz clock frequency ?

d) With proper circuit diagram explain the operation of NMOS NAND gate. 3 + 3 + 4 + 5

9. a) Perform the conversion of D flip-flop to J-K flip-flop.

b) What is presettable counter ? Design a MOD-5 counter that counts its natural count sequence from 000 to 100.

c) Distinguish between a ripple counter and synchronous counter. 5 + 8 + 2

10. a) What are the differences between the Decoder and Demultiplexer ?

b) Form a multiplexer tree to give 4X1 MUX from two 2X1 MUX.

c) Show how a 16 input MUX is used to generate the function

$F = (A,B,C,D) = \overline{A}\overline{B}\overline{C}D + BCD + A\overline{B}\overline{C} + AB\overline{C}D$. 5 + 5 + 5

11. a) What are RAM and ROM ? What is the basic difference between EPROM and EEROM ?

b) What is the major difference between the two classes of finite state machines and proper state diagram ?

c) What is Schmitt Trigger ? (2 + 3) + (4 + 4) + 2

END