

Name : .....

Roll No. : .....

Invigilator's Signature : .....

**CS/B.Tech(CSE)/SEM-3/CS-303/2010-11**

**2010-11**

**COMPUTER ORGANIZATION**

Time Allotted : 3 Hours

Full Marks : 70

*The figures in the margin indicate full marks.*

*Candidates are required to give their answers in their own words  
as far as practicable.*

**GROUP - A**

**( Multiple Choice Type Questions )**

1. Choose the correct alternatives for the following :

10 × 1 = 10

- i) From a Source Code, a compiler can detect
  - a) Run-time error
  - b) Logical errors
  - c) Syntax error
  - d) None of these.
- ii) The purpose of ROM in a Computer System is
  - a) to store constant data required for computers own use
  - b) to help reading from memory
  - c) to store application program
  - d) to store 0,s in memory.

CS/B.Tech(CSE)/SEM-3/CS-303/2010-11

iii) Which one does not possess the characteristics of a memory element ?

- a) A toggle switch                      b) A lamp
- c) An AND gate                          d) None of these.

iv) Data from memory location after fetching is deposited by memory in

- a) MAR                                      b) MBR
- c) IR                                        d) Status Register.

v) How many minimum, NAND gates are required to make a flip-flop ?

- a) 4    b) 3
- c) 2    d) 5.

vi) Virtual memory system allows the employment of

- a) More than address space
- b) The full address space
- c) More than hard disk capacity
- d) None of these.

CS/B.Tech(CSE)/SEM-3/CS-303/2010-11

vii) A system has 48-bit virtual address, 36-bit physical address and 128 MB main memory. How many virtual and physical pages can the address space support ?

- a)  $2^{36}$ ,  $2^{24}$
- b)  $2^{12}$ ,  $2^{36}$
- c)  $2^{24}$ ,  $2^{34}$
- d)  $2^{34}$ ,  $2^{36}$

viii) A UART is an example of

- a) serial asynchronous data transmission ship
- b) PIO
- c) DMA controller
- d) none of these.

ix) A priority interrupt may be accomplished by

- a) Polling
- b) Daisy chain
- c) Parallel method of priority interrupt
- d) All of these.

CS/B.Tech(CSE)/SEM-3/CS-303/2010-11

- x) Control program memory can be reduced by
- a) Horizontal format
  - b) Vertical format micro-program
  - c) Hardwired control unit
  - d) None of these.

**GROUP - B**

**( Short Answer Type Questions )**

Answer any *three* of the following.  $3 \times 5 = 15$

2. a) A digital computer has a common bus system for 16 registers of 32-bits each. The bus is constructed with multiplexers.

- i) How many selection inputs are there in each multiplexer ?
- ii) What size of multiplexers are needed ?
- iii) How many multiplexers are there in the bus ?

- b) Why do most computers have a Common bus system ?

$3 + 2$

3. Draw the logic diagram of a common bus which connects 4 registers of 4-bit each using tristate buffers. 5

CS/B.Tech(CSE)/SEM-3/CS-303/2010-11

4. What is virtual memory ? Why is it called virtual ? Write the advantages of virtual memory. 2 + 1 + 2
5. What is programmed I/O technique ? Why is it not very useful ? 3 + 2
6. Draw the block diagram and explain the functionality of micro-programmed control unit. 5

**GROUP - C**

**( Long Answer Type Questions )**

Answer any *three* of the following.  $3 \times 15 = 45$

7. a) Explain the difference between associative & set associative cache mapping technique.
- b) With the help of following information, determine the size of sub-fields ( in bits ) in the address for Direct mapping, Associative mapping & Set associative mapping :
  - 512 MB main memory & 2 MB cache memory
  - The address space of this processor is 256 MB
  - The block size is 256 bytes
  - There are 16 blocks in a cache set.
- c) Briefly explain the two write policies, write through and write back for cache design. What are we getting the advantages and disadvantages of both the methods ?4 + 6 + 5

CS/B.Tech(CSE)/SEM-3/CS-303/2010-11

8. a) With the help of suitable diagram, explain the advantage of carry look ahead adder over conventional parallel adder.
- b) If a CPU has 8-bit data bus & 16-bit address bus draw the connection diagram for this CPU with 4 256\*8 RAM & 1 512\*8 ROM.
- c) Show the bus connection with a CPU to connect four RAM chips of size  $256 \times 8$ -bits each and a ROM chip of  $512 \times 8$ -bits size. Assume the CPU has 8-bit data bus and 16-bit address bus. Clearly specify generation of chip select signals.
- d) What is dirty bit ?  $5 + 4 + 4 + 2$
9. a) Explain Booth Multiplication Algorithm for signed 2's complement numbers with proper flow-chart. Illustrate this with an example by multiplying  $(-9) \times (-13)$ .
- b) Explain destructive read out & non-destructive read out of memory system.  $(5 + 5) + 5$
10. a) Explain non-restoring division algorithm and explain the hardware diagram. Perform the Restoring division operation with 19 divided by 8.
- b) What is belady's anomaly for page replacement technique ? Explain with example.  $(3 + 2 + 5) + 5$

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CS/B.Tech(CSE)/SEM-3/CS-303/2010-11

11. a) What are the different types of DMA controllers & how do they differ in their functioning ?
- b) Explain the basic DMA operations for transfer of data between memory & peripherals.
- c) Differentiate between memory mapped I/O & I/O mapped I/O.

5 + 5 + 5

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