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2013

COMPUTER ORGANIZATION

Hours | Full Marks : 70

ures in the margin indicate full marks.
quired to give their answers in their own words as far as practicable.

GROUP – A
ltiple Choice Type Questions)

correct alternatives for the following : 10 × 1 = 10

memory

ncreases performance

ncreases machine cycle

reduces performance

none of these.

he basic principle of a Von Neumann computer is

storing program and data in separate memory

b) using pipeline concept

c) storing both program and data in the same memory

d) using a large number of register.

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iii) BIOS is

a) a collection of I/O driver programs

b) part of OS to perform I/O operation

c) firmware consisting of I/O driver programs

d) a program to control one of the I/O peripherals.

iv) Conversion of $(FAFAFA)_{16}$ into Octal form is

a) 767676 b) 76575372

c) 76737672 d) 76727672.

v) Associative memory is

a) content addressable memory

b) pointer addressable memory

c) slow memory

d) none of these.

vi) How many address bits are required for a 1024×8 memory ?

a) 1024 b) 8

c) 10 d) 20.

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If you convert (+46·5) into a 24 bit floating point binary number following IEEE convention, what would be the ...ent ?

...00011100 b) 0000011

...100010 d) none of these.

...ic circuit in ALU is

...entirely combinational

...combinational cum sequential

...entirely sequential

...none of these.

...of virtual memory is equivalent to the size of

...main memory b) cache memmory

...secondary memory d) both (a) and (c).

Which of the following address modes is used in the instruction 'POP B' ?

a) Immediate b) Register

c) Direct d) Register indirect.

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GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. a) Write three points to differentiate memory mapped I/O and I/O mapped I/O.

   b) What are the advantages of Interrupt I/O over programmed I/O ? 3 + 2

3. a) Represent (–9·50) in 64 bit IEEE floating point representation.

   b) What are 'write through' and 'write back' policies in cache memory ? 2 + 3

4. Differentiate between three-address, two-address, one-address and zero-address instructions with suitable example.

5. Compare RISC and CISC architectures in brief. Explain PC-relative addressing mode with example. 3 + 2

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

6. a) Write down the type of addressing modes. Explain with examples.

   b) Draw and explain the instruction state cycle.

A computer uses a memory unit with 256 K words of **32 bits each**. A binary instruction code is stored in one **word of memory**. The instruction has four parts; an **indirect bit**, an operation code, a register code part to **specify one of** 64 registers, and an address part.

How many bits are there in the operation code, the **register** code part, and the address part ?

Draw the instruction word format and indicate the **number** of bits in each part.

How many bits are there in the data and address **inputs** of the memory ? 5 + 4 + 6

Draw the internal cell diagram of SRAM cell.

What is cache memory ? What do you mean by hit ratio **and** ?

According to the following information determine the **format of** subfields (bits) in the address for Associative, **Direct and** Set associative mapping schemes :

256 MB main memory and 1 MB cache memory

Block size = 128 bytes; and there are 8 sets in a block.

Draw and explain memory hierarchy pyramid.

3 + 3 + 6 + 3

8. a) A computer has a main memory of 64K × 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words.
   * How many bits are there in tag, index, block and word fields ?
   * What is the size of one cache word ?
   * How many blocks can be accommodated in the cache ?

   b) A processor's TLB has a hit ratio of 80% and it takes 20 ns to search the TLB and 100 ns to access main memory. What will be the effective access time ?

   c) What is meant by "pipeline architecture" ? How does it improve the speed of execution of processor ?

6 + 4 + (2 + 3)

9. a) Show the bus connection with a CPU to connect four RAM chips of size 256 × 8 bits each and a ROM chip of 512 × 8 bit size. Assume that CPU has 8-bit data bus and 16 bit address bus. Clearly specify generation of chip select signals.

   b) Why do peripherals need interface circuits with them ?

Explain with diagram the daisy chaining priority **interrupt** technique.

Draw a block diagram to illustrate the basic **organisation** of computer system and explain functions **of each unit.** 5 + 2 + 3 + 5