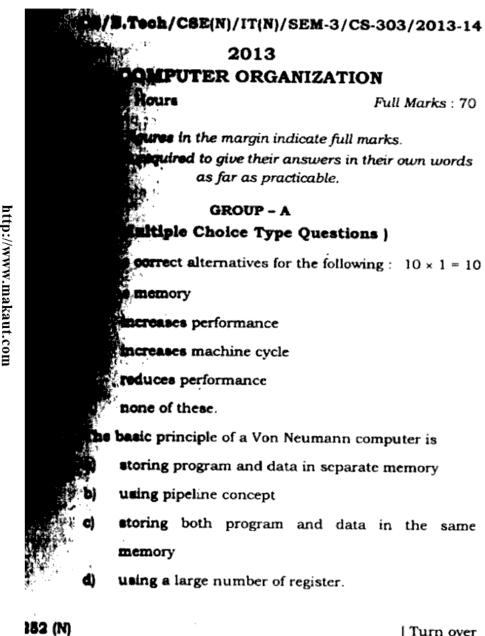
http://www.makaut.com

http://www.makaut.com



| Turn over

CS/B.Tech/CSE(N)/IT(N)/SEM-3/CS-303/2013-14

http://www.makaut.com

iii) BIOS is

- a) a collection of I/O driver programs
- b) part of OS to perform I/O operation
- c) firmware consisting of I/O driver programs
- d) a program to control one of the I/O peripherals.
- iv) Conversion of (FAFAFA)₁₆ into Octal form is
 - a) 767676

b) 76575372

c) 76737672

d) 76727672.

http://www.makaut.com

2 (N)

- v) Associative memory is
 - a) content addressable memory
 - b) pointer addressable memory
 - c) slow memory
 - d) none of these.
- vi) How many address bits are required for a

1024 × 8 memory ?

a) 1024

b) 8

c) 10

d) 20.

3252 (N)

2

http://www.makaut.com

CS/B.Tech/CSE(N)/IT(N)/SEM-3/CS-303/2013-14 If you convert (+46.5) into a 24 bit floating point binary number following IEEE convention, what would be the **50001**1100 0000011 **100**010 none of these. ide circuit in ALU is entirely combinational combinational cum sequential entirely sequential none of these. of virtual memory is equivalent to the size of main memory cache memmory secondary memory both (a) and (c). Which of the following address modes is used in the Instruction 'POP B'? **Immediate** b) Register Direct Register indirect.

3 | Turn over http://www.makaut.com

GROUP - B

(Short Answer Type Questions)

Answer any three of the following. $3 \times 5 = 15$

- a) Write three points to differentiate memory mapped I/O and I/O mapped I/O.
 - b) What are the advantages of Interrupt I/O over programmed I/O?
- 3. a) Represent (-9.50) in 64 bit IEEE floating point representation.
 - b) What are 'write through' and 'write back' policies in cache memory?
- Differentiate between three-address, two-address, oneaddress and zero-address instructions with suitable example.
- Compare RISC and CISC architectures in brief. Explain
 PC-relative addressing mode with example.

GROUP - C

(Long Answer Type Questions)

Answer any three of the following. $3 \times 15 = 45$

- a) Write down the type of addressing modes. Explain with examples.
 - b) Draw and explain the instruction state cycle.

A computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one of memory. The instruction has four parts; an tit, an operation code, a register code part to one of 64 registers, and an address part.

now many bits are there in the operation code, the code part, and the address part?

Praw the instruction word format and indicate the **immer** of bits in each part.

How many bits are there in the data and address aputs of the memory?

5 + 4 + 6

the internal cell diagram of SRAM cell.

is cache memory? What do you mean by hit ratio

of subfields (bits) in the address for Associative,

256 MB main memory and 1 MB cache memory

260 MB main memory and 1 MB cache memory

260 MB main memory and 1 MB cache memory

260 MB main memory and 1 MB cache memory

260 MB main memory and 1 MB cache memory

5

3+3+6+3

- A computer has a main memory of 64K × 16 and a cache memory of 1K words. The cache uses direct mapping with a block size of 4 words.
 - * How many bits are there in tag, index, block and word fields?
 - * What is the size of one cache word?
 - * How many blocks can be accommodated in the cache?
 - b) A processor's TLB has a hit ratio of 80% and it takes 20 ns to search the TLB and 100 ns to access main memory. What will be the effective access time?
 - c) What is meant by "pipeline architecture" ? How does it improve the speed of execution of processor ?

$$6 + 4 + (2 + 3)$$

- 9. a) Show the bus connection with a CPU to connect four RAM chips of size 256 x 8 bits each and a ROM chip of 512 x 8 bit size. Assume that CPU has 8-bit data bus and 16 bit address bus. Clearly specify generation of chip select signals.
 - b) Why do peripherals need interface circuits with them?

interrupt technique.

a block diagram to illustrate the basic elements of computer system and explain functions 5+2+3+5