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Paper Code : PCC-CS-302

PUID : 03444 (To be mentioned to the main answer script)

COMPUTER ORGANISATION

Time Allotted : 3 Hours | *Full Marks* : 70

The figures in the margin indicate full marks.

Candidates are required to give their answers in their own words as far as practicable.

GROUP – A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for any *ten* of the following : $10 \times 1 = 10$

   i) A source program is usually in

      a) Assembly language

      b) Machine level language

      c) High-level language

      d) Natural language.

   ii) In straight binary code, N-bits or N binary digits can represent ..... different values.

      a) 2^N b) 2^(N + 1)

      c) 2^(N-1) d) 2^N-1.

iii) Maximum n bit 2's complement number is

a) 2^n b) 2^n-1

c) $2^{(n-1)}-1$ d) Cannot be said.

iv) The addressing mode, where you directly specify the operand value is

a) Immediate b) Direct

c) Definite d) Relative.

v) How is the effective address of base-register calculated ?

a) By addition of base register contents to the partial address in instruction

b) By addition of implied register contents to the partial address in instruction

c) By addition of base register contents to the complete address in instruction

d) By addition of implied register contents to the complete address in instruction.

vi) The instruction, Add R1, 45 does

a) Adds the value of 45 to the address of R1 and stores 45 in that address.

b) Adds 45 to the value of R1 and stores it in R1

c) Finds the memory location 45 and adds that content to that of R1

d) None of these.

vii) A 24 bit address generates an address space of ..... locations.

a) 1024
b) 4096
c) 2^{48}
d) 16,777,216.

viii) What could be the maximum size of onchip cache memory for an n-address bit processor ?

a) 0
b) 2^n
c) infinite
d) decided by manufacturer.

ix) To get the physical address from the logical address generated by CPU we use

a) MAR
b) MMU
c) Overlays
d) TLB.

x) The contention for the usage of a hardware device is called

a) structural hazard
b) stalk
c) deadlock
d) none of these.

xi) The periods of time when the unit is idle is called as

a) Stalls

b) Bubbles

c) Hazards

d) Both Stalls and Bubbles.

xii) The DMA transfer is initiated by

a) Processor

b) The process being executed

c) I/O devices

d) OS.

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. How can a full adder be implemented using half adders ? Explain with proper circuit diagram.

3. Explain the different kinds of data hazards in pipelining with suitable examples.

4. a) Briefly explain IEEE 754 format for floating point representation of numbers.

b) Represent the decimal value-12.5 in IEEE single precision format.

5. a) If a direct mapped cache has a hit rate of 95%, a hit time of 4ns, and a miss penalty of 100ns, what is the average memory access time ?

b) If an L2 cache is added with a hit time of 20ns and a hit rate of 50%, what is the new average memory access time ?

GROUP – C
(Long Answer Type Questions)

Answer any *three* of the following. 3 × 15 = 45

6. Write short notes on the following :

a) Restoring Division Algorithm

b) Direct Memory Access

c) IEEE double precision format.

7. a) Explain the difference between full associative and direct mapping technique.

b) Explain the write back and write through policies in cache.

c) Cache memory has 2K blocks. Block size is of 4 words = 16 bytes. 32 bit address is provided. The machine is byte addressable.

i) What is the bit length for each field in Direct Mapping ?

ii) What is the bit length for each field in 2-way set associative mapping ?

iii) What is the bit length for each field in 4-way set associative mapping ?

8. a) What is the difference between isolated I/O and memory mapped I/O ?

b) Explain Cache Coherence.

c) Explain the different hazards in pipelining.

9. a) What are the different addressing modes ?

b) Explain with suitable examples of each of the modes.

c) Evaluate the following arithmetic expression into (i) three address, (ii) two address, (iii) one address and (iv) zero address instruction format

$X = (A + B)^* (C + D)$.

10. a) What are the differences between RISC and CISC ?

b) Divide 43 by 11 using Non-restoring algorithm (The tracing table must be shown clearly)

c) What is meant by overflow and underflow in signed magnitude representation of numbers ?